WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

an MFMIS transistor including a first field effect transistor and a ferroelectric capacitor formed on or above said first field effect transistor with a gate electrode of said first field effect transistor working as or being electrically connected to a lower electrode of said ferroelectric capacitor, an upper electrode of said ferroelectric capacitor working as a control gate and said first field effect transistor having a first well region; and

a second field effect transistor having a second well region that is isolated from said first well region of said first field effect transistor,

wherein said first well region of said first field effect transistor is electrically connected to a source region of said second field effect transistor, and

said gate electrode of said first field effect transistor is electrically connected to a drain region of said second field effect transistor.

2. The semiconductor memory of Claim 1,

wherein said first field effect transistor, said second field effect transistor and a driving circuit for driving said first and second field effect transistors are formed on one semiconductor substrate, and

a driving voltage supplied to said driving circuit and

a DC voltage supplied to said second well region of said second field effect transistor are supplied from one voltage supply.

3. The semiconductor memory of Claim 1,

wherein said first well region of said first field effect transistor and said second well region of said second field effect transistor have different conductivity types.

4. A method for driving a semiconductor memory composed of an MFMIS transistor including a first field effect transistor and a ferroelectric capacitor formed on or above said first field effect transistor with a gate electrode of said first field effect transistor working as or being electrically connected to a lower electrode of said ferroelectric capacitor, an upper electrode of said ferroelectric capacitor working as a control gate and said first field effect transistor having a first well region, and a second field effect transistor having a second well region that is isolated from said first well region of said first field effect transistor, said first well region of said first field effect transistor being electrically connected to a source region of said second field effect transistor and said gate electrode of said first field effect transistor being electrically connected to a drain region of said second field effect transistor, comprising the steps of:

writing a data in said MFMIS transistor by applying a

voltage between said control gate and said first well region of said first field effect transistor with said second field effect transistor placed in an on-state; and

reading a data from said MFMIS transistor by detecting change of channel resistance of said first field effect transistor with said second field effect transistor placed in an off-state.

5. The method for driving a semiconductor memory of Claim 4,

wherein a driving voltage supplied to a driving circuit for driving said first and second field effect transistors and a DC voltage supplied to said second well region of said second field effect transistor are supplied by one voltage supply.

6. The method for driving a semiconductor memory of Claim 4,

wherein said first well region and said second well region have different conductivity types.